Notice of Allowability	Application No.	Applicant(s)	
	09/159,748	BARRETT, GEOFF	
	Examiner	Art Unit	
	Thomas H. Stevens	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed 12/12/2005*.

2. ☒ The allowed claim(s) is/are *1-17*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. Claims 1-11 were previously examined.

2. Claims 12-17 were added.

3. Claims 1-17 were examined.

Section I: New Examiner

4. Tom Stevens is presiding over the prosecution in place of William Thomson.

Section II: Allowable Subject Matter

5. Claims 1-17 are allowed.

6. The following is an examiner's statement of reasons for allowance:

While Kimura-S., "Residue BDD and Its Application to the Verification of Arithmetic Circuits" teaches (claim 1) a method of ordering variables of a binary decision diagram representation of a hardware system, comprising acts of: arranging the variables of the binary decision diagram in a representation of a graph corresponding to the hardware system; Cockett et al., "Decision Tree Reduction" teaches (claims 1,3 and 7) the graph having a top, nodes and leaves, the nodes being labeled with the variables of the binary decision diagram and the leaves, whereby the set of functions labeling the leaves reachable from one of the nodes corresponds to the set of functions that depend on the variables labeling the one of the nodes; traversing the representation of the graph from the top down to produce a list of labels in a selected order; (claim 7) representing the hardware system as a binary decision diagram having a plurality of nodes, the nodes being labeled with variables to provide labels for the node; US Patent US 5,243,538

teaches (claim 2) an apparatus for ordering variables of a binary decision diagram representation of a hardware system, comprising; a first storage circuit to store first bits representing the variables of the binary decision diagram; a second storage circuit; and a processor, coupled to the first storage circuit and the second storage circuit, programmed to (claims 2, 7 and 8) arrange the variables of the binary decision diagram in a representation of a graph having a top, nodes, and leaves, and to generate labels for the nodes and leaves, the nodes being labeled with the variables of the binary decision diagram and the leaves being labeled with a set of functions, the set of functions labeling the leaves reachable from one of the nodes corresponding to the set of functions which depend on the variables labeling the one of the nodes, the processor also being programmed to traverse the representation of the graph from the top down, and to output to the second storage circuit a list of labels in a selected order based; (claim 6) storage circuitry for storing bits representative of a set of functions as a binary decision diagram corresponding to the hardware system, the binary decision diagram having a plurality of nodes, the nodes being labeled with variables to provide labels for the nodes; (claims 7 and 8) a method for providing the properties of a hardware system comprising a plurality of internal signals, wherein a plurality of functions determine variables of the internal signals; an apparatus for providing properties of a hardware system, the hardware system comprising a plurality of internal signals, wherein a plurality of functions determines the values of the internal signals, none of these references, taken either alone or in combination, with the prior art of record discloses

(claim 1) "using the selected order of the list to determine a sifting order in which the variables are to be shifted to restructure the binary decision diagram representation of the hardware system prior to sifting the variables,"

(claims 2 and 7) "representation of the graph prior to the sifting the variables according to the select order,"

(claim 3) "A method of restructuring a binary decision diagram representative...based on the act of sifting the variables,"

(claim 6) "An apparatus for restructuring a binary decision diagram representative, a processor adaptive to detect a number of nodes of the binary decision diagram, and in response to the diction,"

(claim 8) "first storage circuitry for storing bits representative of a set of functions which represent the hardware; second storage circuitry, wherein the sifted variables of the binary decision diagram are written by the processor to the second storage circuitry,"

in combination with the remaining elements and features of the claimed invention. It is for these reasons that the applicants' invention defines over the prior art of record. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany

the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (8:00 am- 4:30 pm EST).

If attempts to reach the examiner by telephone are unsuccessful, please contact examiner's supervisor Mr. Paul Rodriguez 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.. Answers to questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) (toll-free (866-217-9197)).

March 27, 2006

TS

Paul L. Rodriguez 4/3/06
Primary Examiner
Art Unit 2125 2127